

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re the Application of:

Naoki YADA et al.

Appln. No.:

Filed: Herewith

For: MICROCOMPUTER, PROGRAMMING METHOD AND ERASING METHOD

* * *

PRELIMINARY AMENDMENT

Assistant Commissioner for Patents
Washington, D.C. 20231

Sir:

Prior to examination, please amend the above-identified
patent application as indicated below.

IN THE CLAIMS:

Please amend Claims 3, 5 and 9 as set forth below.

- 1 3. (Amended) The microcomputer according to claim 1,
- 2 further including second register means (FKEY) readable and
- 3 writable by said CPU, and

4 wherein said non-volatile memory sets the setting of a
5 second set value to said second register means as a necessary
6 condition for enabling erase and programming operations, and
7 said CPU sets a value other than the second set value to
8 said second register means upon said branch and sets the
9 second set value to said second register means for each return
10 from the branch.

1 5. (Amended) The microcomputer according to claim 1,
2 further including an interrupt control circuit for inputting
3 an interrupt request signal therein, and performing
4 arbitration of interrupt requests which compete with one
5 another, and an interrupt priority level-based interrupt mask
6 process to thereby output an interrupt signal to said CPU, and
7 wherein said CPU causes said interrupt control circuit to
8 carry out a setting for masking an interrupt lower in
9 interrupt priority level than a non-maskable interrupt.

1 9. (Amended) The microcomputer according to claim 7,
2 further including a RAM disposed in an address space of said
3 CPU, and

4 wherein said non-volatile memory has a transfer control
5 program for transferring the erase and program control program
6 to said RAM, and said CPU sets parameters for said another
7 process to the erase and program control program transferred
8 to said RAM, based on the set value of the first register
9 means and thereby executes the erase and program control
10 program.

 Please add the following claims:

1 40. (New) The microcomputer according to claim 2,
2 further including second register means (FKEY) readable and
3 writable by said CPU, and
4 wherein said non-volatile memory sets the setting of a
5 second set value to said second register means as a necessary
6 condition for enabling erase and programming operations, and
7 said CPU sets a value other than the second set value to
8 said second register means upon said branch and sets the
9 second set value to said second register means for each return
10 from the branch.

1 41. (New) The microcomputer according to claim 40,
2 wherein the value other than the second set value is code
3 information indicative of the progress of an erase and program
4 process.

1 42. (New) The microcomputer according to claim 2,
2 further including an interrupt control circuit for inputting
3 an interrupt request signal therein, and performing
4 arbitration of interrupt requests which compete with one
5 another, and an interrupt priority level-based interrupt mask
6 process to thereby output an interrupt signal to said CPU, and
7 wherein said CPU causes said interrupt control circuit to
8 carry out a setting for masking an interrupt lower in
9 interrupt priority level than a non-maskable interrupt.

1 43. (New) The microcomputer according to claim 42,
2 wherein said CPU executes a process for changing the location
3 of an interrupt process routine for a non-maskable interrupt
4 request to an address of a RAM upon execution of the erase and
5 programming.

1 44. (New) The microcomputer according to claim 8,
2 further including a RAM disposed in an address space of said
3 CPU, and

4 wherein said non-volatile memory has a transfer control
5 program for transferring the erase and program control program
6 to said RAM, and said CPU sets parameters for said another
7 process to the erase and program control program transferred
8 to said RAM, based on the set value of the first register
9 means and thereby executes the erase and program control
10 program.

REMARKS

Claims 3, 5, and 9 have been amended to avoid the multiple dependent claim surcharge. Claims 40-44 presented herein correspond to the dependencies eliminated from the amended claims.

The Commissioner is hereby authorized to charge to Deposit Account No. 50-1165 any fees that may be required by this paper and to credit any overpayment to that Account.

Respectfully submitted,

MWS:sjk

By: 

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MARKED-UP VERSION OF THE CLAIMS:

1 3. (Amended) The microcomputer according to claim 1 [or
2 2], further including second register means (FKEY) readable
3 and writable by said CPU, and

4 wherein said non-volatile memory sets the setting of a
5 second set value to said second register means as a necessary
6 condition for enabling erase and programming operations, and

7 said CPU sets a value other than the second set value to
8 said second register means upon said branch and sets the
9 second set value to said second register means for each return
10 from the branch.

1 5. (Amended) The microcomputer according to claim 1 [or
2 2], further including an interrupt control circuit for
3 inputting an interrupt request signal therein, and performing
4 arbitration of interrupt requests which compete with one
5 another, and an interrupt priority level-based interrupt mask
6 process to thereby output an interrupt signal to said CPU, and

7 wherein said CPU causes said interrupt control circuit to
8 carry out a setting for masking an interrupt lower in
9 interrupt priority level than a non-maskable interrupt.

1 9. (Amended) The microcomputer according to claim 7 [or
2 8], further including a RAM disposed in an address space of
3 said CPU, and
4 wherein said non-volatile memory has a transfer control
5 program for transferring the erase and program control program
6 to said RAM, and said CPU sets parameters for said another
7 process to the erase and program control program transferred
8 to said RAM, based on the set value of the first register
9 means and thereby executes the erase and program control
10 program.